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Thermo-mechanical Stress in Through-Silicon-Vias

1. Introduction

During the last several years, the enhancement of integrated circuits (ICs) performance and power consumption have contributed to the continual scaling down the size of transistors. However, scaling down semiconductor devices has brought serious challenges to the materials and processes of on-chip interconnects beyond the 32-nm technology node. Therefore, some researchers proposed another direction to increase the device density by making ICs into three-dimensional (3D) spaces and the 3D IC stacking has attracted tremendous attention for IC integration in order to reduce wire length and footprint.

Through silicon via (TSV) is regarded as the best choice of the connection between wafer and wafer. By using TSVs in 3D integration, the system performance can be significantly improved and the manufacturing cost is reduced. However, there are still some challenges in this technology.

The major reliability concern has to do with the high thermal expansion mismatch stresses caused by the dissimilar materials of the high expansion copper (Cu) and low expansion silicon (Si). These thermal stresses, which are ubiquitously induced during processing and thermal cycling of TSV structures, can potentially degrade the performance of stress-sensitive devices around the TSVs or drive crack growth in 3D interconnects. Therefore, the success of 3D integration largely relies on the thermo-mechanical stresses developed in the system and its impact on reliability.

Finite element methods have been widely used to numerically analyze the thermo-mechanical stresses in 3D structures and regarded as the only conceivable approach for analyzing and characterizing stress in circuits accompanied with complicated structures. Silvaco tools, especially Victory Process, can be used for 3D TSV stress simulation. In this article, an analytical approach based on classical Lame problem in elasticity was used to verify 3D FEM solutions from Victory Process.

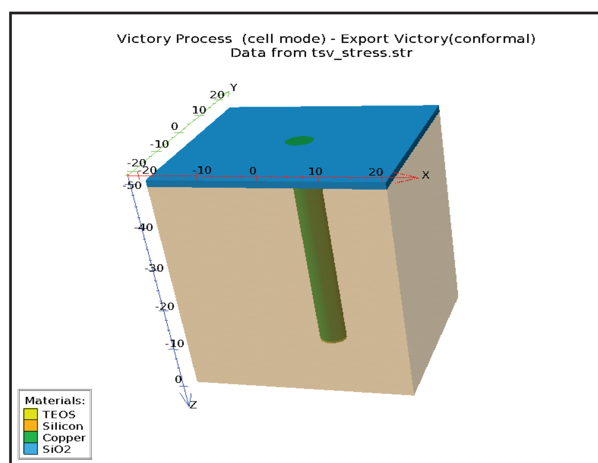

Figure 1. A single TSV embedded in Si.

2. Verification

2.1 Analytical Approach

The cylindrical TSV is easy to manufacture and became one of the most commonly used structures. Consider a single cylindrical TSV embedded in Si wafer [Figure 1], and the system is subjected to a uniform thermal loading (ΔT). As a prerequisite for the verification, we assume that all materials are isotropic and linearly elastic.

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If the Si wafer is large enough in all three directions, the exact solution to this problem is identical to the 2D plane strain solution to the classical Lame problem in elasticity [1]. The stress in the via is uniform and tri-axial with the following components:

$$\sigma_r = \sigma_\theta = \frac{-E_f \varepsilon_T}{1 - 2\upsilon_f + \frac{1+\upsilon_m}{1+\upsilon_f}\frac{E_f}{E_m}} \quad (1)$$

$$\sigma_z = -E_f \varepsilon_T \left(\frac{1 + \frac{1+\upsilon_m}{1+\upsilon_f}\frac{E_f}{E_m}}{1 - 2\upsilon_f + \frac{1+\upsilon_m}{1+\upsilon_f}\frac{E_f}{E_m}}\right) \quad (2)$$

where σ_r, σ_0 and σ_z are the radial, circumferential (hoop) and axial stresses, respectively, and $\varepsilon T = (\alpha_f - \alpha_m)\Delta T$ is the mismatch strain due to a thermal load T. The material properties, α, E and υ are the coefficient of thermal expansion (CTE), Young's modulus and Poisson's ratio, with the subscripts f and m for the via (fiber) and Si (matrix), respectively. On the other hand, the corresponding stress field in Si ($r > D_f = 2$) is nonuniform and bi-axial

$$\sigma_r = -\sigma_\theta = \frac{-E_f \varepsilon_T}{1 - 2\upsilon_f + \frac{1+\upsilon_m}{1+\upsilon_f}\frac{E_f}{E_m}} \cdot \left(\frac{D_f}{2r}\right)^2 \quad (3)$$

where D_f is the diameter of the TSV and r is the radial coordinate measured from the center of the via.

The stress field induced by differential thermal expansion in the via and Si is 3D in nature. If we ignore the elastic mismatch between the via and Si by setting $E_f = E_m = E$ and $\upsilon_f = \upsilon_m = \upsilon$, the 3D stresses along the depth at the center of the via ($r = 0$) can be obtained in closed form as follows [1]:

$$\sigma_z(z) = -\frac{E\varepsilon_T}{1-\upsilon}\frac{z^3}{(z^2 + \frac{D_f^2}{4})^{\frac{3}{2}}} \quad (4)$$

$$\sigma_r(z) = \sigma_\theta(z) = -\frac{E\varepsilon_T}{2(1-\upsilon)}\left[-2\upsilon + \frac{2(1+\upsilon)z}{(z^2 + \frac{D_f^2}{4})^{\frac{1}{2}}} + \frac{z^3}{(z^2 + \frac{D_f^2}{4})^{\frac{3}{2}}}\right] \quad (5)$$

The variation of the stresses in the via is important for the study of plastic yielding and stress migration in TSVs.

2.2 Stress Simulation

To verify with the analytic solution given in the previous section, FEA is performed using Stress statement in Victory Process. By defining TSV layout parameters, such as TSV diameter, TSV pitch and TSV count, an automated layout is generated in Victory Process followed by 3D cell mode structure generation as shown in Figure 1. The model structure has the TSV diameter $D = 5\mu m$ and the wafer thickness $H = 50\mu m$, such that $H/D = 10$. In radial direction, $40\mu m$ $40\mu m$ rectangular Si block is considered. To satisfy large Si wafer assumption, free boundary conditions are imposed in all three directions:

```
STRESS TEMPERATURE=270 T.FINAL=20
   FREE.X FREE.Y FREE.Z
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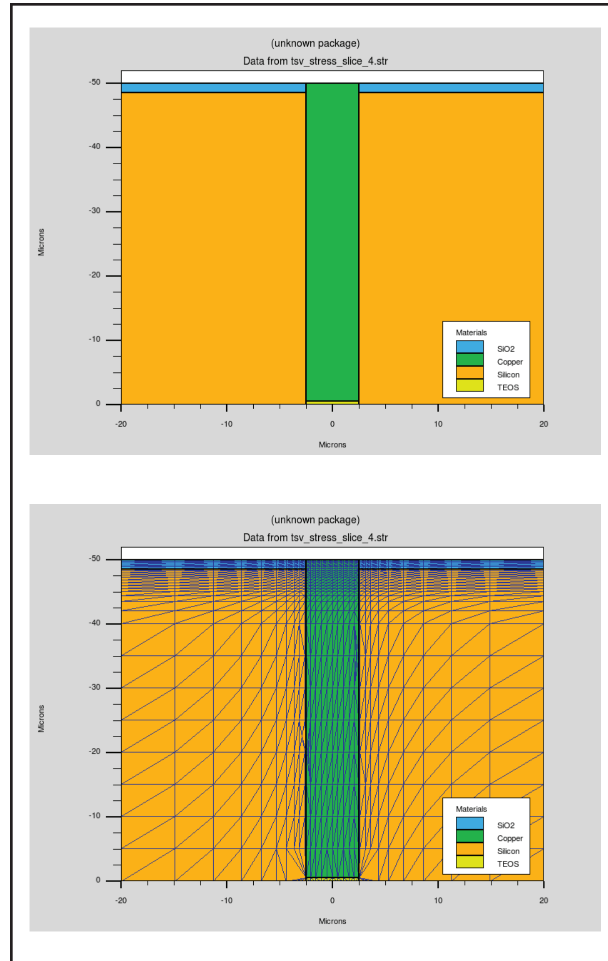


Figure 2. cut-plane view (H/D=10).

Figure 2 shows cut-plane view of the structure, and with mesh lines on the right. As shown in the figure, TEOS liner ($0.5\mu m$) and SiO_2 insulation layer are also included in the model. In practice, a thin barrier layer is typically needed between the Cu via and Si, which has minimal effects on the stress distribution and is thus ignored here.

The material of TSV has different choices, such as Cu, W and poly-crystalline silicon. Currently, Cu is the most commonly used interconnect materials in the integrated circuit since the resistivity of Cu is minimum. In this article, we use Cu as TSV material in order to be compatible with existing technology.

Material	CTE/ppm K^{-1}	Young's modulus/GPa	Poisson's ratio
Si	2.6	130	0.28
Cu	16.5	110	0.34
SiO_2	2.6	130	0.28
TEOS	16.5	110	0.34

Table 1. Material properties (case 1).

2.2.1 Case 1

The first case is to compare simulation with the plane strain solutions given in (3). The Victory Process uses SMDB as its database for default material constants. The material properties of the Si and Cu are extracted from SMDB. To mimic the analytical model, the material properties of SiO_2 is assumed to be the same as Si and TEOS is same as Cu. This is done by modifying SMDB. The material parameters used for this case are shown in Table 1. Thermal load is ΔT = –250C, which is, we assume that the TSV structure is annealed at 270*C* and cooled down to 25C to mimic the manufacturing process. The default AMS iterative solver was used for the 3D stress simulation and could solve the equations within a reasonable amount of run-time (131 seconds on Intel i7 4.55GHz CPU).

Figure 3 shows a comparison of analytical model and finite element simulation: the radial stress contrast and the hoop stress contrast, respectively. The plus sign stands for the tensile stress while the minus sign stands for the compressive stress. The simulation results were extracted at the mid-plane of the wafer (z=H = 0.5). It can be seen from the figure that the error between the analytical model and the nite element model is negligible.

Figure 4 shows the stress profile contour.

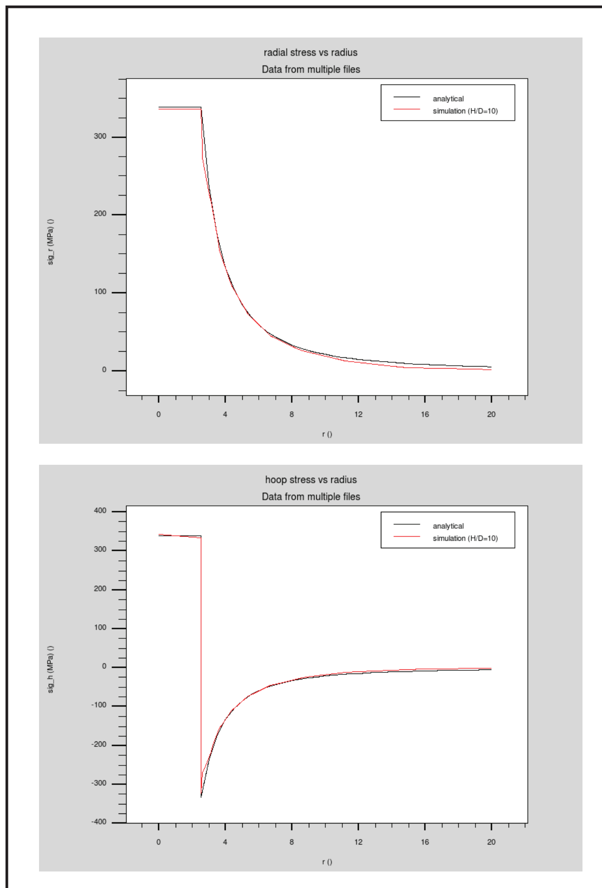


Figure 3. Comparison between analytical model and simulation (case 1).

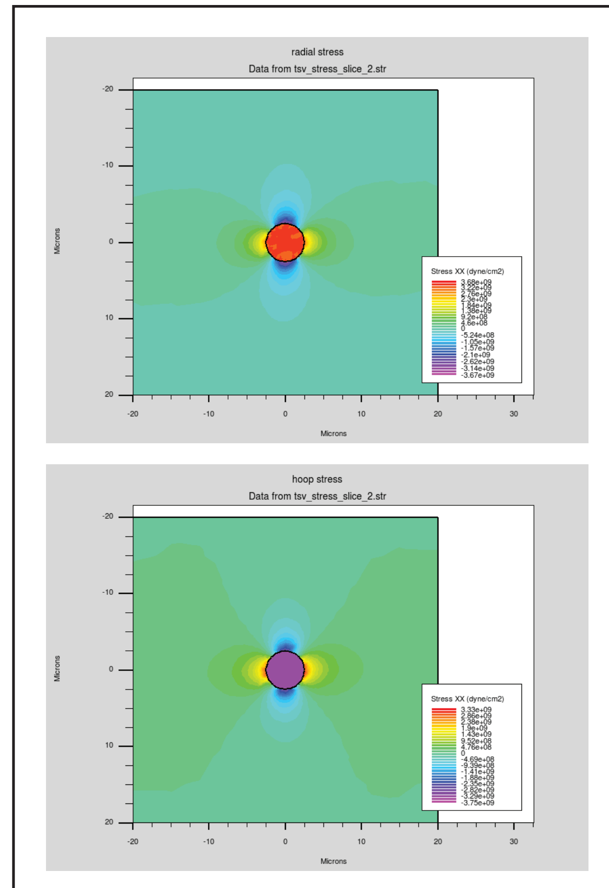


Figure 4. Stress profile contour of the simulation (case 1).

Material	CTE/*ppm* K^{-1}	Young's modulus/GPa	Poisson's ratio
Si	2.3	110	0.35
Cu	17	110	0.35
SiO_2	2.3	110	0.35
TEOS	17	110	0.35

Table 2. Material properties (case 2).

2.2.2 Case 2

In this case, the variation of the stresses in the via along depth is compared. The analytical solution was given in (4) and (5). The elastic mismatch between Cu and Si is neglected for this case. The material parameters used for this case are shown in Table 2. Since the thickness of the Si wafer is one of the key design parameters for the TSV structure, the effect of wafer thickness on thermal stress distribution is examined with two different thicknesses. To this end, an additional structure with $H = 10\mu m$ (H/D=2) is created. The same thermal load (ΔT = –250*C*) is applied.

Figure 5 shows the results, in comparison with the analytical solution. First, the axial stress (σ_z) along the center line of the TSV (r = 0) shows the transition from zero stress at the surface (z = 0) to a tensile stress away

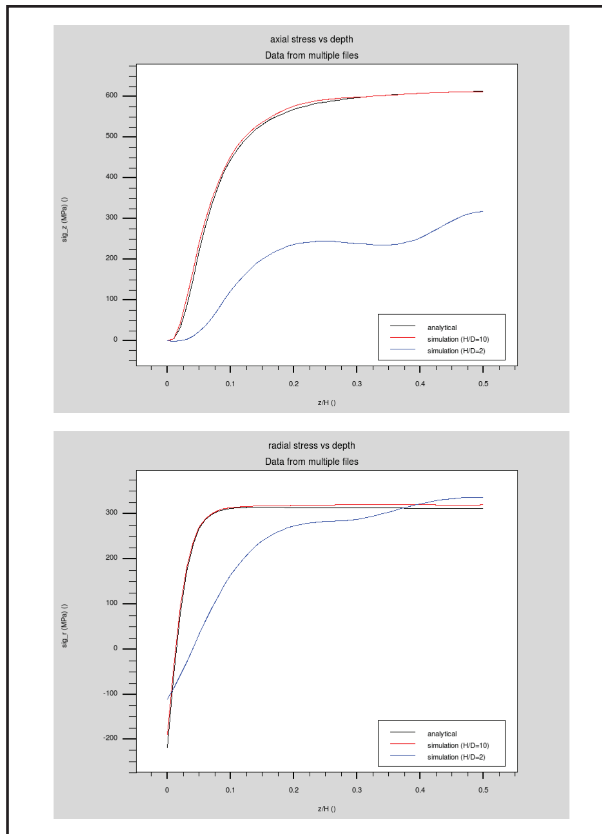


Figure 5. Comparison between analytical model and simulation.

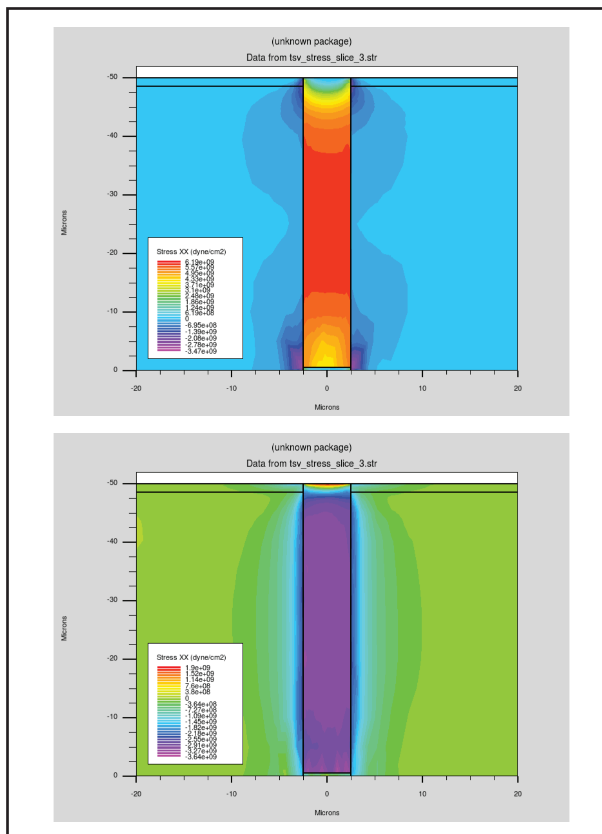


Figure 6. Stress prole contour (case 2).

from the surface (top plot). For the thick wafer (H/D=10), the FEA results show excellent agreement with the analytical solution in (4). For the thin wafer (H/D=2), however, the axial stress in the TSV is significantly lower, due to the close proximity of the two free surfaces.

The radial stress (σ_r) along the center line of the TSV (r = 0) again compares well with the analytical solution in (5) for the thick wafer, but some deviations for the thin wafer (bottom plot). Both radial and axial stresses asymptotically approach to the 2D solution given in (1) and (2) far away from the surface. For the thin wafer, the radial stress is slightly higher near the surface but is lower elsewhere. Figure 6 shows stress profile contour for the thick wafer.

It is seen from Figure 5 that the 2D plane strain solution only predicts stresses far away from the wafer surface, while the analytical 3D solution is a good approximation everywhere for relatively thick wafers (e.g., $H/D > 10$). Neither solution is applicable for relatively thin wafers.

3. Impact of An-isotropic Stresses on TSV Reliability

The mechanical properties of the crystalline materials depend on the orientation of the layout relative to the crystal lattice. This means that the correct values for analyzing two different designs in silicon may differ up to 45%. However, the common practices only do the isotropic calculations because of the perceived complexity of the subject. As a result, many researchers oversimplify silicon elastic behavior and use inaccurate values for design and analysis. The an-isotropic effects are properly taken into account in recent versions of Victory Stress and Victory Process. To access the impact of an-isotropic analysis, we make the model more realistic by having three TSVs in a row. The silicon layer is also 1.5 times deeper than the TSV depth as shown in Figure 7. The an-isotropic calculation is easily invoked in Victory Process by turning on STRESS.ANISO parameter in METHOD statement:

```
method stress.aniso=on
```

All material properties from the built-in material database (SMDB) have been used without any modification. Table 3 shows the material parameters used for the isotropic case.

Material	CTE/*ppm* K^{-1}	Young's modulus/GPa	Poisson's ratio
Si	2.6	130	0.28
Cu	16.5	110	0.34
SiO_2	0.12	66	0.20
TEOS	0.54	20	0.15

Table 3. Material properties for the isotropic case.

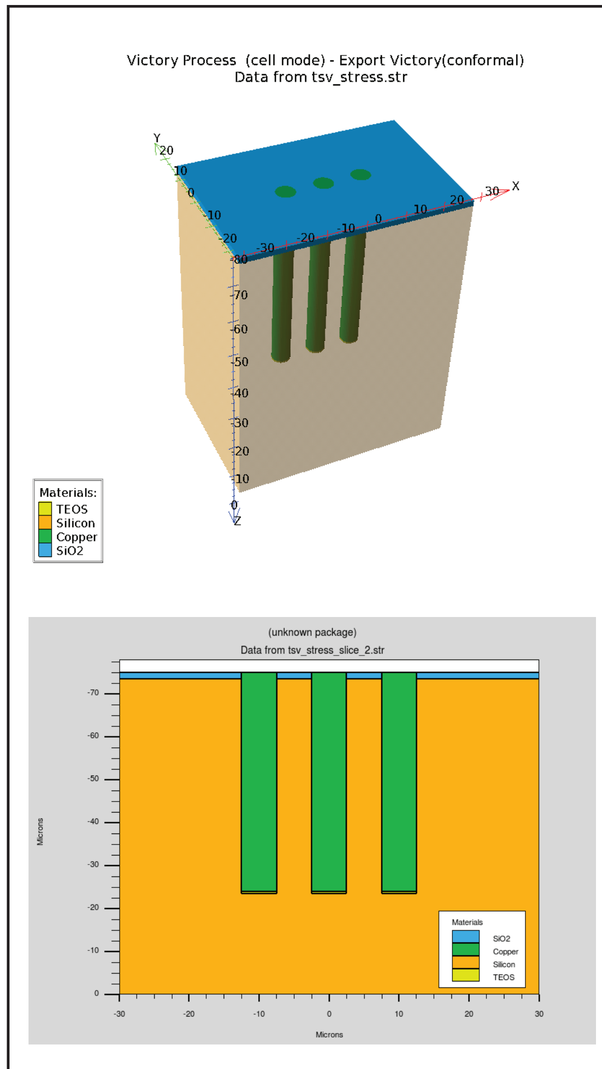


Figure 7. Three TSVs embedded in Si for an-isotropic analysis.

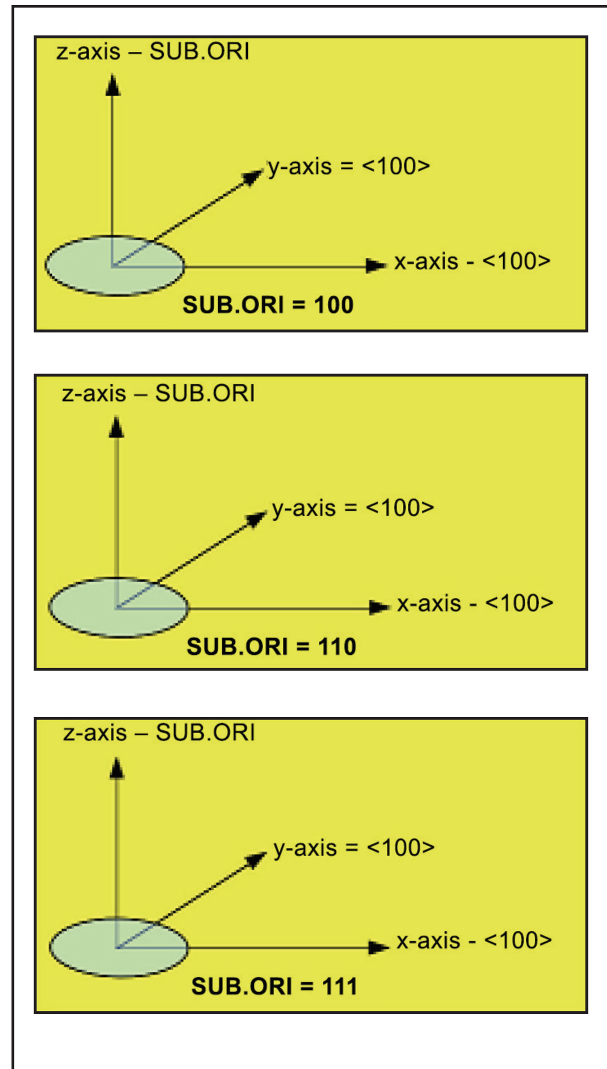


Figure 8. Default orientation of the lattice for diamond crystals.

For the an-isotropic case, silicon is the only an-isotropic material. In a general an-isotropic material, a fourth rank tensor with 81 terms is required to describe the elasticity by relating the second rank tensors of stress and strain. Fortunately, in silicon, the combination of plane symmetry and the equivalence of the shear conditions (cubic crystals) allow us to specify the fourth rank tensor with only three independent constants: c_{11} = 166 GPa, c_{12} = 64 GPa, and $c44$ = 80 GPa.

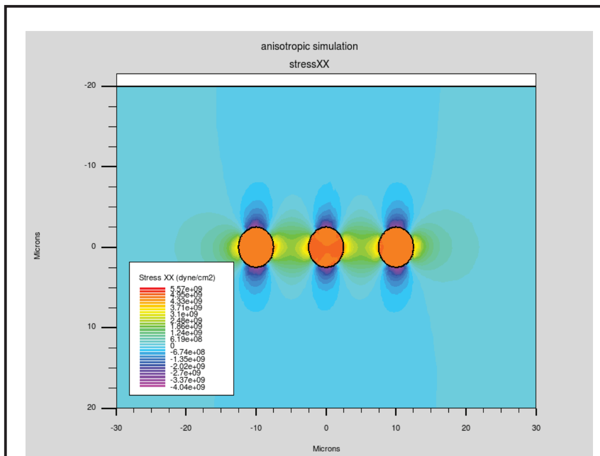
The default substrate orientation <100> has been used for the an-isotropic analysis as shown in Figure 8.

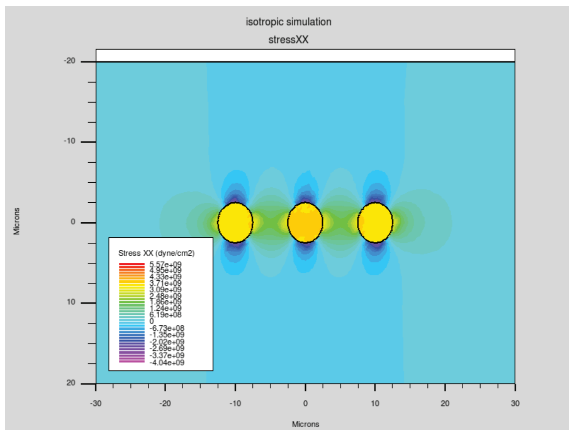
Figure 9 and Figure 10 are contour plot and comparison plot (red line: anisotropic, blue line: isotropic) of stressXX and stressYY, respectively, in the XY cut-plane at z=-37.5. It is clearly shown that the TSV stresses are about 35% higher in as-isotropic case. This indicates that the isotropic analysis underestimates the risk of TSV failure by plastic yielding.

Figure 11 shows the contour of Von Mises stress in XZ cut-plane at y=0. The Von Mises stress along the via/Si interface is important for the study of TSV reliability because the shear stress and the tensile stress contribute to the driving force for interfacial delamination in the case of cooling ($\Delta T < 0$), and the Von Mises stress is a single indicator combining shear and tensile stresses.

Again, the Von Mises stress is about 35% higher in an-isotropic case. This indicates that the isotropic analysis underestimates the risk of interfacial delamination.

Since most of the failures in the TSV result from either plastic yielding or interfacial cracks, an-isotropic analysis provides a proper tool for the assessment of the TSV reliability. For a more detail analysis to decide the failure mechanism and exact failure locations, advanced material constitutive relations such as plasticity and failure model will be required in the future.





(0,0) to (0,20) cut-line plot

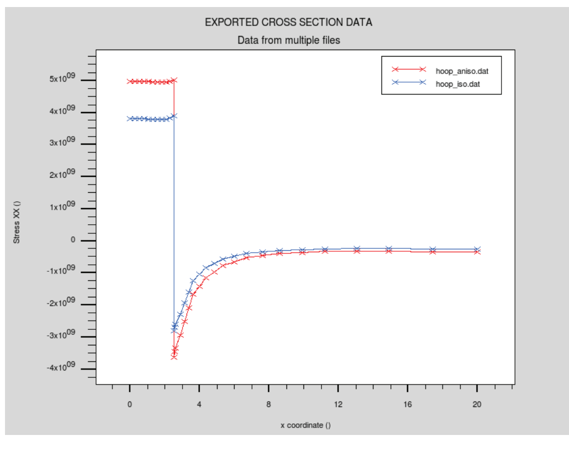
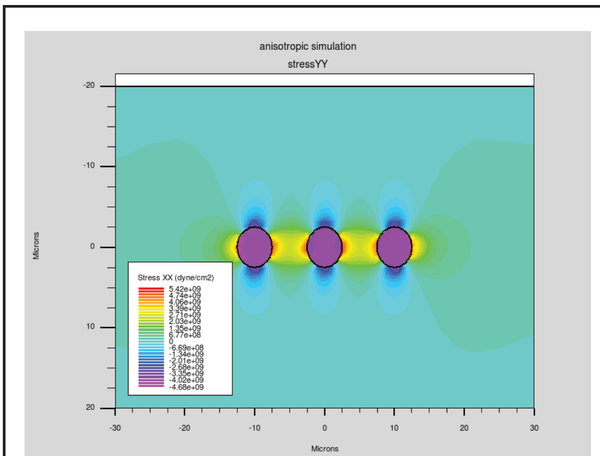
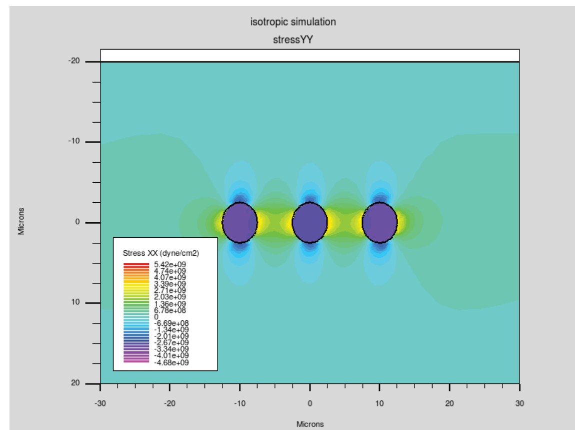


Figure 9. stressXX.





(0,0) to (0,20) cut-line plot

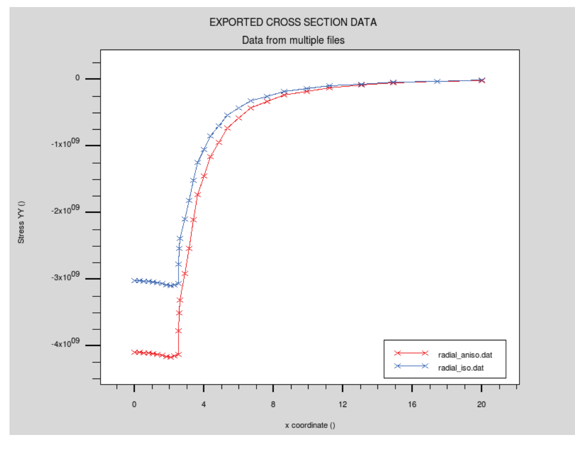
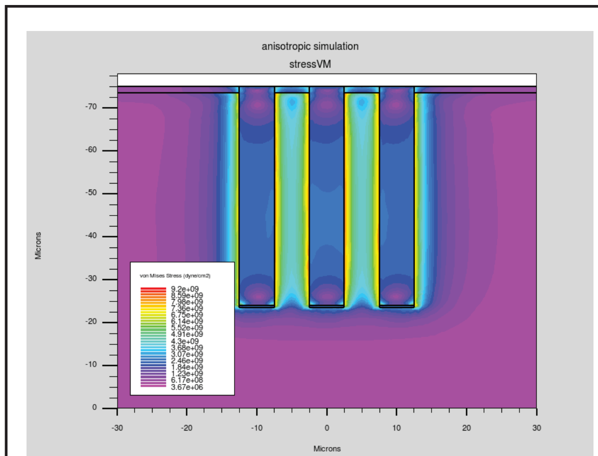
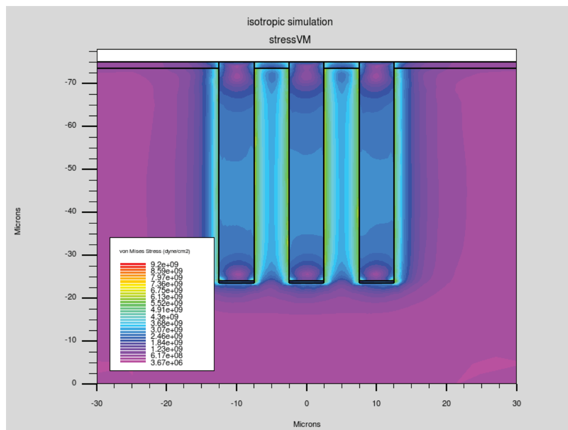


Figure 10. stressYY.





(2.501,-75) to (2.501,-50) cut-line plot

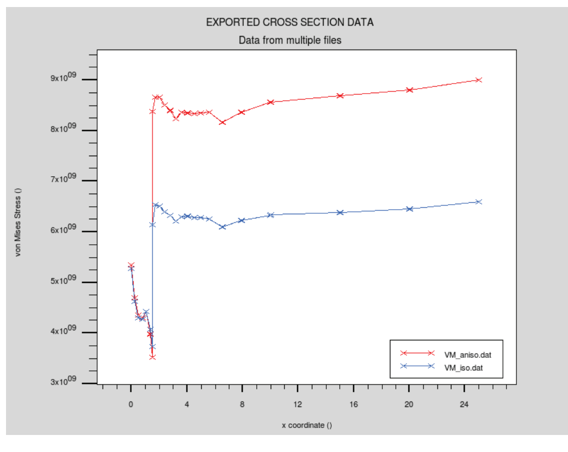


Figure 11. Von Mises stress.

4. Summary

- The thermo-mechanical reliability of a TSV structure in 3D interconnect is investigated by an analytical approach and stress simulation.
- The simulation results compare closely with the analytic solution for the thick wafer. This verifies that Victory Process stress simulation is very reliable.
- The analytic solution, which is given for the large length scale, is not in good agreement with the simulation results for the thin wafer as expected. This means that the near-surface stresses, which are essential for the design as they degrade the electrical performance of the devices located near the surface, can only be reasonably predicted by simulations.
- For the TSV reliability analysis by simulations, taking the an-isotropic characteristics of the silicon into account is very important because the common isotropic analysis substantially underestimate the risk of TSV failure and interfacial delamination.

References

[1] S. Timoshenko and J. N. Goodier, Theory of Elasticity. New York: McGraw-Hill, 1970, pp. 403-407.